In the Claims:

1. (Currently Amended) A system, comprising:

a signal generator coupled to an input of a signal line, the signal generator generating a signal of a particular frequency;

at least one receiving device electrically coupled to an output of the signal line, wherein the at least one receiving device comprises a clock generator, wherein the clock generator is synchronized to the signal and generates a clock signal, wherein the clock signal comprises a frequency less than a frequency of the signal of [[a]] the particular frequency; and

an impedance element coupled to the input of the signal line, the impedance element comprising an impedance chosen to create a resonant condition at the input of the signal line, wherein the resonant condition comprises a resonant frequency that essentially coincides with the frequency of the signal.

2. (Previously Presented) The system according to Claim 1, wherein the signal is essentially sinusoid.

3. (Previously Presented) The system according to Claim 1, wherein the signal generator comprises a driver device.

4. (Previously Presented) The system according to Claim 1, wherein the signal generator generates an essentially rectangular signal.

5. (Currently Amended) The system according to Claim 4, wherein the essentially rectangular signal generated by the ~~driver device~~ signal generator is filtered, wherein a signal present at an input node of the signal line is essentially sinusoid.

6. (Previously Presented) The system according to Claim 1, wherein the impedance element comprises an inductive component.

7. (Currently Amended) The system according to ~~claim~~ Claim 6, wherein the impedance element comprises a capacitive component.

8. (Currently Amended) The system according to Claim 7, wherein an inductance of the inductive component and/or [[the]] a capacitance of the capacitive component is set during a manufacture of the system.

9. (Currently Amended) [[A]] The system according to Claim 8, wherein the inductance and/or capacitance is variably adjustable after the manufacture of the system.

10. (Previously Presented) The system according to Claim 9, wherein the capacitive component comprises a capacitive diode.

11. (Previously Presented) The system according to Claim 1, wherein the at least one receiving device comprises a semi-conductor component.

12. (Currently Amended) The system according to Claim 1, wherein the at least one receiving device uses the signal for chronological co-ordination of relaying and/or processing and/or ~~transfer~~ transfering of data.

13. (Currently Amended) The system according to Claim 1, wherein the at least one receiving device ~~device~~ generates a further signal under control of the signal, wherein the further signal is used for chronological co-ordination of relaying and/or processing and/or ~~transfer~~ transferring of data.

14. (Previously Presented) The system according to Claim 13, wherein the further signal comprises a lower frequency than the signal.

15. (Previously Presented) The system according to Claim 14, wherein the at least one receiving device comprises a PLL or DLL circuit, wherein the PLL or DLL circuit generates the further signal.

16. (Currently Amended) A process for generating a synchronizer, the process comprising:

transmitting a signal from a signal generator device coupled to an input of a signal line to at least one receiving device coupled to an output of the signal line in an electronic system, wherein the signal line comprises a capacitive load;

coupling at least one additional device at an output of the signal generator, the at least one additional device comprising an impedance such that a resonant-oscillatory condition is created at [[an]] the output of the signal generator;

adjusting a center frequency of the resonant-oscillatory condition, wherein the center

frequency is modified to essentially coincide with a frequency of the signal; and

generating a clock signal synchronized to the signal, wherein a frequency of the clock signal is less than the frequency of the signal, and wherein the clock signal is generated by the at least one receiving device.

17. (Previously Presented) The process of claim 16, wherein the adjusting the center frequency comprises switching on or off at least one additional device coupled to the output of the signal generator.

18. (Previously Presented) The process of claim 17, wherein the at least one additional device comprises a capacitive diode.

19. (Currently Amended) The process of claim 17, wherein [[that]] the at least one additional device comprises at least two additional devices, the at least two additional devices being connected in parallel.